

## Multi-pass pipelining: Enhancing In-Order Microarchitectures to Out-of-Order Performance

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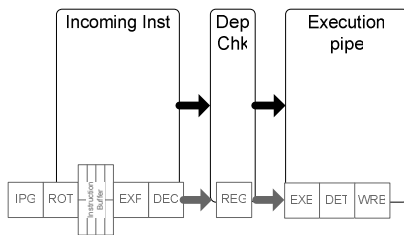
## Dynamic scheduling approach:

- Finding ILP at runtime comes at heavy cost
- Out-of-order execution incompatible with overriding power/power density concerns
  - ALPHA21264—18% of chip power, as much as int + fp exec
  - POWER4—10% of core power, scheduler highest power density
- Power concerns influencing development towards less speculative, lower frequency designs (Pentium M)

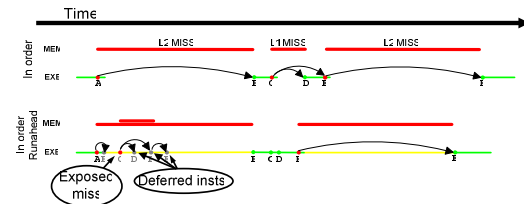
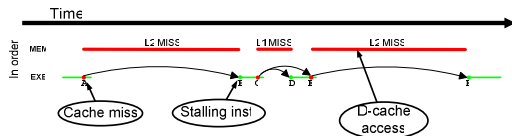
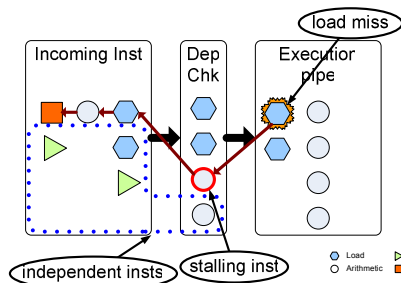
## EPIC approach:

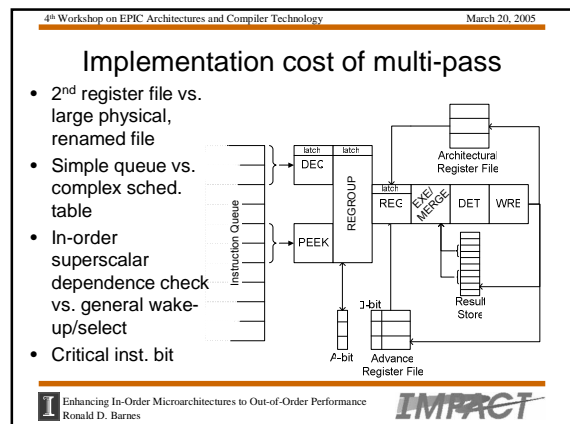
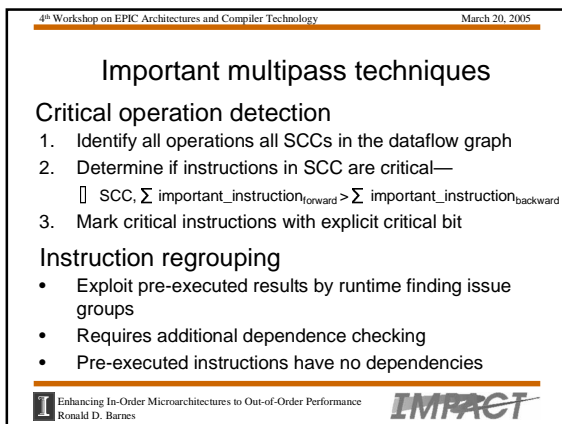
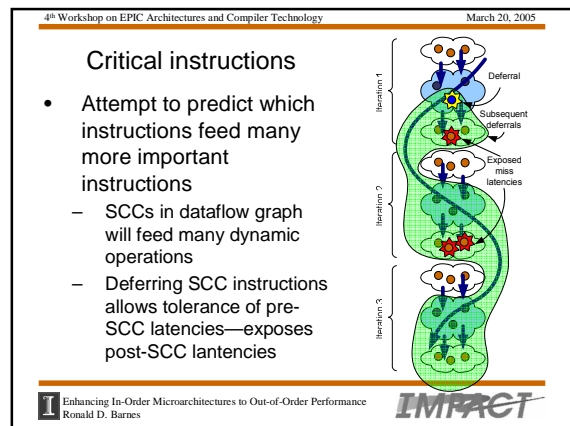
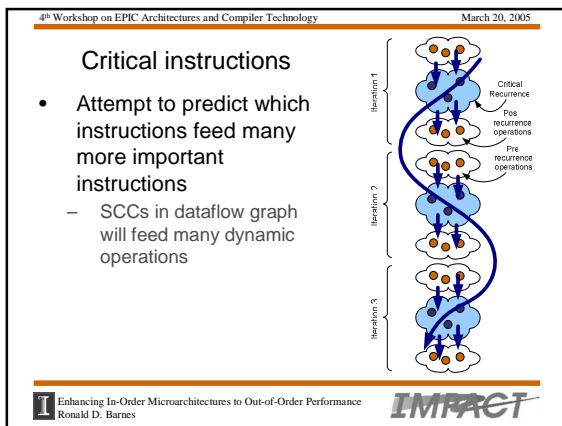
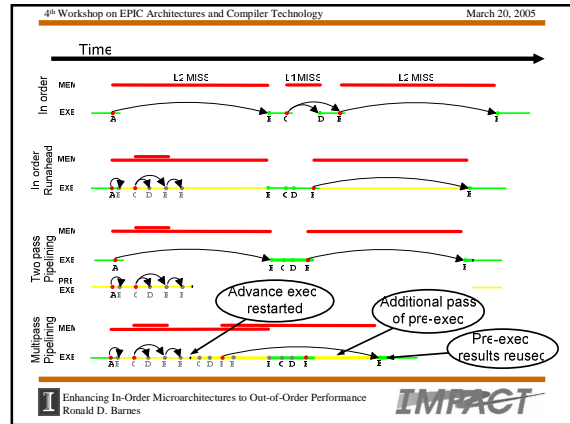
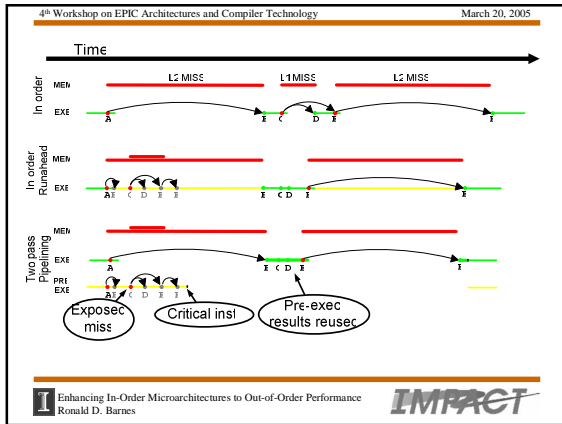
- Compiler-planned execution—scalable approach
- Compiler techniques (e.g. prefetching) not solving problem of unanticipated memory latency

## In-order pipeline



## In-order cache-stall problem



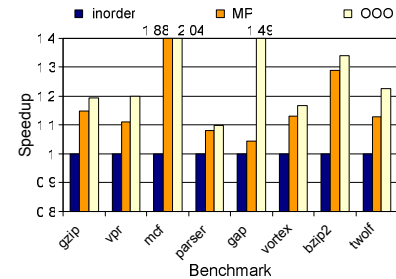


## Experimental configuration

Feature	Parameters
Functional Units	6-issue, Itanium II FUs
L1I Cache	1 cycles, 16 KB, 4-way, 64 B lines
L1D Cache	1 cycles, 16 KB, 4-way, 64 B lines
L2 Cache	5 cycles, 256 KB, 4-way, 128 B lines
L3 Cache	12 cycles, 1.5 MB, 12-way, 128 B lines
Main Memory	145 cycles
Data model	32-bit Integers, Longs and Pointers
Issue Queue	256 entry

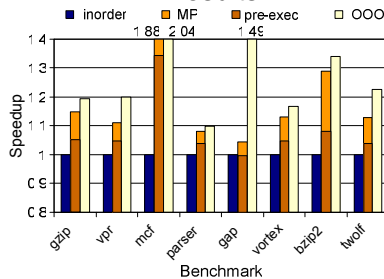
- Benchmarks compiled with IMPACT C compiler using control-flow profiling and interprocedural alias analysis
  - Profile-driven inlining, hyperblock formation and control-speculation

## Results



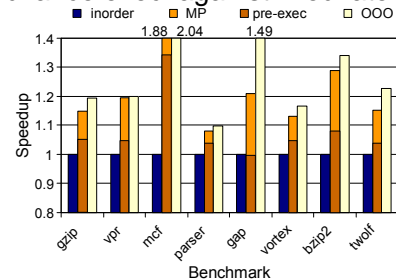
- Achieves 78% of OOO cycle reduction (excluding gap)

## Results



- MP reduces 2.7X cycles as simple pre-execution

## Advance exec. against fixed latencies



- OoO only 1.05X speedup over multipass

## Conclusion

- Variations in anticipated latency of memory instructions significantly impact in-order performance
- Multi-pass execution provides an cache-miss latency tolerant microarchitecture
- Instruction regrouping achieves significant benefit from reusing results of pre-executed instructions
  - In contrast to OoO runahead [Mutlu05]